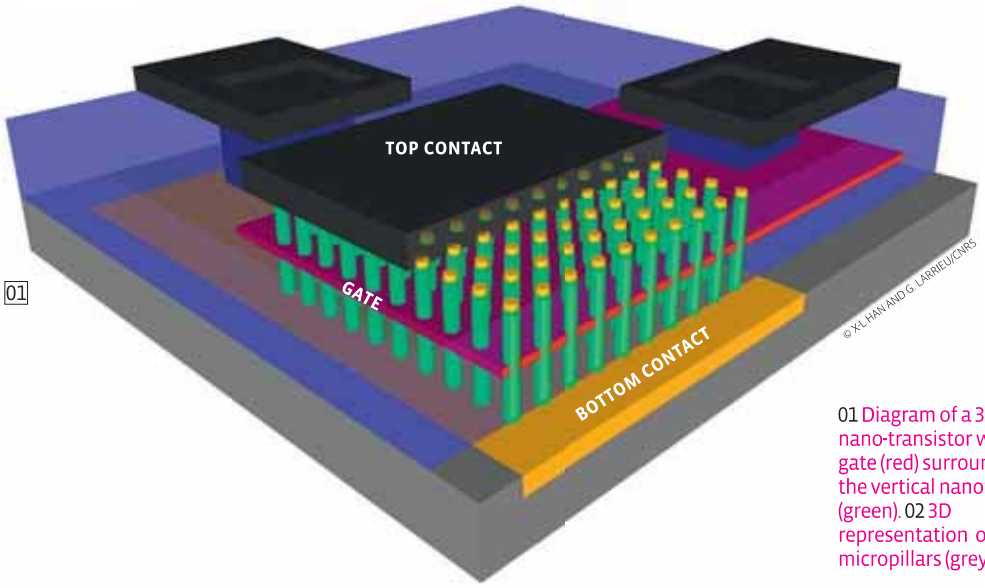
Computer Science Using vertical nanowire transistors and the directed growth of actin filaments, CNRS leads the effort in miniaturization and 3D computer circuitry.

3D Transistors for Faster Computers

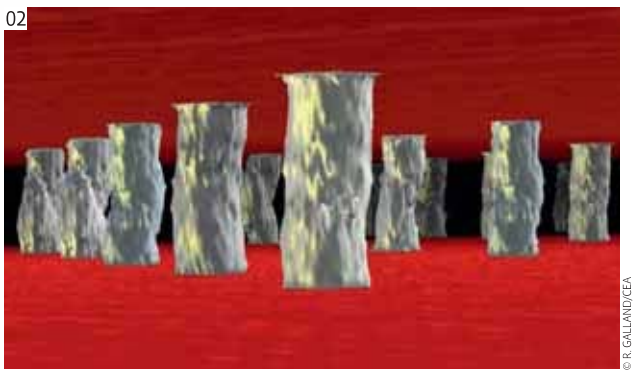
01



01 Diagram of a 3D nano-transistor with the gate (red) surrounding the vertical nanowires (green). 02 3D representation of actin micropillars (grey).

BY BRETT KRAABEL

02



Since its invention, the transistor has been a flat device with its three electrical components (source, drain, and gate) coexisting on a single plane. In the race to increase computing power, this planar architecture was not an issue since transistors could continuously be made smaller. Yet they have now become so small that further shrinking is impossible without degrading their performance, and a paradigm shift in chip architecture is required. This is being spearheaded by several research teams at CNRS and takes the form of 3D transistors and chip circuitry.

Guilhem Larrieu at the LAAS[1] and his colleague Xiang-Lei Han from the IEMN[2] were able to create 3D transistors in the form of vertical nanowire arrays.[3] Each nanowire acts as a mini transistor with the source at one end and the drain at the other. The crucial element is the gate, which controls whether or not current passes through the transistor. For vertical-nanowire arrays, the gate consists of a horizontal 14-nm-thick layer of metal pierced by all the nanowires of the array. A section of each nanowire is thus fully surrounded by the metal gate, forming the "gate-all-around" architecture. As Larrieu explains, "it's easier to control the flow of water through a hose by pinching it from all sides than by pressing only one side." Besides giving the transistor excellent electrical properties, this approach actually simplifies the manufacturing process.

Another logical approach to overcome planar miniaturization is to start building up, by stacking transistors above one another, which requires vertical circuitry. To do this, a team from the LPCV[4] led by Laurent Blanchoin and Manuel Théry grew actin filaments to create vertical fibers between horizontal planes.[5] They then coated these fibers with gold to make them conductive.

This approach stems from the study of cell morphogenesis, which involves the growth of actin filaments. "After we controlled actin growth in two dimensions," recalls Blanchoin, "our colleagues in techno asked for 3D structures because the real challenge in this field is to connect chips in 3D." The method they developed uses lasers to draw nucleation sites on two opposite internal surfaces. Upon injecting a mixture of actin monomer and proteins between these surfaces, actin polymerization occurs at the nucleation sites. The result is that the actin fibers grow perpendicular to the surfaces and adopt the geometry of their nucleation sites.

These two highly-promising research avenues could prove essential for increased miniaturization and pave the way for greater computing power and lower energy consumption.

01. Laboratoire d'analyse et d'architecture des systèmes (CNRS).
02. Institut d'électronique, de microélectronique et de nanotechnologie (CNRS / Universités Lille-I and Valenciennes / ISEN Lille / Ecole centrale de Lille).
03. G. Larrieu et al., "Vertical nanowire array-based field effect transistors for ultimate scaling," *Nanoscale*, 2013. 5: 2437–41.
04. Laboratoire de physiologie cellulaire et végétale (CNRS / CEA / INRA / UJF).
05. R. Galland et al., "Fabrication of three-dimensional electrical connections by means of directed actin self-organization," *Nat. Mat.*, 2013. 12: 416–21.

CONTACT INFORMATION:
LAAS, Toulouse.
Guilhem Larrieu
› guilhem.larrieu@laas.fr
iRTSV-LPC&V, Grenoble.
Laurent Blanchoin
› laurent.blanchoin@cea.fr
Manuel Théry
› manuel.thery@cea.fr